Logic and memory concepts for all-magnetic computing based on transverse domain walls

This content has been downloaded from IOPscience. Please scroll down to see the full text.

View the table of contents for this issue, or go to the journal homepage for more

Download details:
IP Address: 157.193.82.35
This content was downloaded on 01/12/2015 at 12:26

Please note that terms and conditions apply.
Logic and memory concepts for all-magnetic computing based on transverse domain walls

J Vandermeulen\(^1\), B Van de Wiele\(^1\), L Dupré\(^1\) and B Van Waeyenberge\(^2\)

\(^1\) Department of Electrical Energy, Systems and Automation, Ghent University, Sint Pietersnieuwstraat 41, B-9000 Ghent, Belgium
\(^2\) Department of Solid State Sciences, Ghent University, Krijgslaan 281-S1, B-9000 Ghent, Belgium

E-mail: jasper.vandermeulen@ugent.be

Received 26 February 2015, revised 5 May 2015
Accepted for publication 14 May 2015
Published 9 June 2015

Abstract
We introduce a non-volatile digital logic and memory concept in which the binary data is stored in the transverse magnetic domain walls present in in-plane magnetized nanowires with sufficiently small cross sectional dimensions. We assign the digital bit to the two possible orientations of the transverse domain wall. Numerical proofs-of-concept are presented for a NOT-, AND- and OR-gate, a FAN-out as well as a reading and writing device. Contrary to the chirality based vortex domain wall logic gates introduced in Omari and Hayward (2014 Phys. Rev. Appl. 2 044001), the presented concepts remain applicable when miniaturized and are driven by electrical currents, making the technology compatible with the in-plane racetrack memory concept. The individual devices can be easily combined to logic networks working with clock speeds that scale linearly with decreasing design dimensions. This opens opportunities to an all-magnetic computing technology where the digital data is stored and processed under the same magnetic representation.

Keywords: transverse domain wall, magnetic nanowires, all-magnetic computing, logic gates, magnetic memory

(Some figures may appear in colour only in the online journal)
components per chip leading to a high processing speed and a reduced power consumption. While magnetic field driven logic elements were experimentally demonstrated [6], current driven alternatives would be preferable with respect to miniaturization. Indeed, while magnetic fields are highly nonlocal in nature, the effect of electric currents is restricted to the nanowire to which they are applied. Moreover, since the magnetic domain (wall) dynamics depends on the current density [7], power consumption scales down when reducing cross sectional dimensions.

Very recently, Omari et al [8] proposed to use the magnetic domain walls rather than the magnetic domains to store the digital data. In particular, in in-plane magnetized nanowires with sufficiently large cross sectional dimensions vortex domain walls exist [9] of which the chirality (clockwise or counter clockwise) can represent the digital data. They introduced numerical prototypes for logic gates and a fan-out system. Such domain wall technologies are promising as the digital bit. We give numerical proofs-of-concept for logic elements, a fan-out system as well as a reading and writing device. In all components, localized spin polarized currents drive the domain wall motion and control the domain wall bit, making our concepts complementary to the magnetic domain wall based memory and logic technology in which the shape of pinning sites and nanowire widths. These aspects hinder miniaturization. Moreover, we show that our concepts are relatively robust against geometrical inaccuracies. Envisaged clock speeds scale proportional with cross-sectional dimensions enabling a straight forward design of logic networks. Moreover, we show that our concepts are relatively robust against geometrical inaccuracies. Envisaged clock speeds scale proportional with cross-sectional dimensions enabling a straight forward design of logic networks.

The propagation of the vortex domain walls and the manipulation of their chirality is driven by magnetic fields. Also, vortex domain walls can not exist in magnetic nanowires with reduced cross sectional dimensions. Furthermore, the functioning of the proposed designs is very sensitive to dimensions of pinning sites and nanowire widths. These aspects hinder miniaturization. Moreover, their numerical designs require a Gilbert damping increased by about one order of magnitude to 0.5, increasing the intrinsic magnetic losses proportionally. Furthermore, despite several experimental investigations [10–12], Omari et al mention that methods for controllably injecting and sensing vortex domain walls have not yet been fully developed. Based on their simulations, they envisage a clock speed of 50–100 MHz.

In this paper, we introduce an alternative magnetic domain wall based memory and logic technology in which the shape of the transverse domain wall present in in-plane magnetized magnetic nanowires with reduced cross sectional dimensions [9] represents the digital bit. We give numerical proofs-of-concept for logic elements, a fan-out system as well as a reading and writing device. In all components, localized spin polarized currents drive the domain wall motion and control the domain wall bit, making our concepts complementary to the magnetic domain wall based memory and logic technology in which the shape of pinning sites and nanowire widths. These aspects hinder miniaturization. Contrary to [8], all designs have input and output nanowires with identical cross sectional dimensions enabling a straight forward design of logic networks. Moreover, we show that our concepts are relatively robust against geometrical inaccuracies. Envisaged clock speeds scale proportional with miniaturization starting from a clock speed of about 66 MHz for the presented elements with 100 nm wide nanowires.

2. Methodology

Transverse domain wall based digital elements are numerically designed using the micromagnetic software package MuMax [13, 14] considering Permalloy nanowires with characteristic material parameters: saturation magnetization \( M_{\text{sat}} = 860 \times 10^3 \text{ A m}^{-1} \), exchange stiffness \( k_{\text{ex}} = 1.3 \times 10^{-11} \text{ J m}^{-1} \), Gilbert damping \( \alpha = 0.02 \), zero anisotropy and a degree of non-adiabaticity \( \xi = 0.04 \). A polarization \( P = 0.5 \) of the electrical current is used. All input and output nanowires have 10 nm × 100 nm cross sectional dimensions. In general discretization cells with sizes 3.125 × 3.125 × 10 nm are used. For the sensitivity analysis of the notch geometry discretization cells have dimensions 1.5625 × 1.5625 × 10 nm.
Figure 1(a) shows the four possible domain walls in the Permalloy nanowire. The characteristic triangular shape of the transverse domain walls results from the competition between demagnetizing and exchange interactions [9]. We assign a digit 1 to the V-orientation and a digit 0 to the \( \Lambda \)-orientation of the wall. As both orientations are equally stable they are a valid candidate to store the digital bit. Contrary to magnetic fields, electrical currents applied along the wire axis move all domain walls (bits) into the same direction ensuring the functionality of the logic designs for both tail-to-tail and head-to-head transverse domain walls. The domain wall velocity versus applied current density \( j \) is illustrated in figure 1(b). The local maximum defines the Walker breakdown current density \( j_w \). For current densities \( j < j_w \), the domain wall moves along the wire with a constant speed proportional to the current density without changing its shape, see figure 1(c). For current densities \( j > j_w \), the domain wall continuously changes its orientation \( V \rightarrow \Lambda \rightarrow V \rightarrow \ldots \). Here, the domain wall velocity is not constant in time leading to a reduced average velocity, see figure 1(d). In terms of the envisaged transverse domain wall based technology this means that for current densities below \( j_w \) the digital data is fixed and moving at a constant speed while above \( j_w \) the digital data is moving and continuously changing its bit value. In our numerical designs we incorporated space varying current densities computed with COMSOL multiphysics.

3. Logical gates

3.1. NOT-gate

A NOT-gate, or inverter, is a basic logic element that converts a logic ‘0’ into a logic ‘1’ and vice versa. In our approach, this translates into reverting the domain wall orientation. As this naturally happens when applying a current density \( j > j_w \), see figure 1(d), NOT-gate functioning can be accomplished by locally tailoring the Walker breakdown properties. A possible NOT-gate design is presented in figure 2(a). The material properties have been adjusted over a length \( L \), such that the Walker breakdown current density \( j_w \) is reduced in this part of the nanowire. Several material as well as geometrical parameters (e.g. wire width and thickness, disorder [15]) can be locally changed to create such an effect. We chose to vary the Gilbert damping, see figure 2(b). When applying a current density \( j < j_w \), one can obtain one single switch of the domain wall orientation—\( V \) to \( \Lambda \) or vice versa—if the length \( L \) allows so. Figure 2(c) shows that NOT-gate functioning is obtained over a wide range of \( j \sim L \) combinations, proving the robustness of the design.

Doping with rare-earth metals can be used to vary the damping parameter \( \alpha \) in the nanowire [16, 17]. An increase in \( \alpha \) of 0.01 can be achieved by adding an atomic concentration of 20, 0.26, 0.28, or 0.59 percent of respectively
Gd, Tb, Dy, or Ho to the Permalloy material, as estimated from [17].

3.2. AND- and OR-gate

The AND-gate implements logical conjunction, while the OR-gate implements logical disjunction. A possible design of an AND-gate with two domain wall bits at its input channels is presented in figure 3. In both input nanowires a current density $j=j_0$ is injected to move the domain walls. From figures 3(b)–(e) it is clear that the functionality of the device depends on the domain wall bit arriving first at the junction (region III): when the domain wall bit in the bottom input nanowire arrives first, OR-gate functionality is obtained while AND-gate functionality is obtained when the domain wall bit in the top input nanowire arrives first. Similar behavior was observed by Omari et al in their design of e.g. a NAND gate.

In our design, the first arriving domain wall bit pins at the junction itself and at additional notches highlighted in figure 3(a) by the purple boxes. At the arrival of the second bit, the resulting two-domain wall complex depins and combines to the output domain wall bit. The depinning dynamics for all possible combinations of input (head-to-head) domain wall bits, depending on the arrival sequence is shown in figures 3(b)–(e). One can qualitatively understand the depinning dynamics by interpreting how the magnetic flux runs through the DW structures. In panels (b) and (c) identical input bits naturally merge to the same output bit, preserving the flux direction present in the input bits. The domain wall bits in panel (d) have their vertex of the V or $\Lambda$ shape pinned at the notch and their flux expands over the complete junction area. This flux forces the last arriving domain wall to switch its magnetization direction by means of an intermediate antivortex state, adding enough energy to depin the domain wall complex. In panel (e) the first domain wall bit has its vertex pinned at the junction, introducing a more localized flux, barely influencing the magnetization orientation in the secondly arriving domain wall bit. The arrival of the second domain wall bit again depins the system, now forming an unstable antivortex domain wall with a core polarization corresponding to the out-of-plane tilting direction of the pinned domain wall. It is known that, when a spin-polarized current is applied to the domain wall, it is tilted out-of-plane [18]. The same is valid for a trapped domain wall, where the spin torque is balanced by an out-of-plane tilting, as can be seen from the generalized 1D model [19]. Similar to vortex domain walls [20],

Figure 3. (a) Possible design of an AND-gate. The OR-gate design has the delay element (depicted by the green delineated area) in the top input nanowire (region I). Black circles (regions I and IV) highlight pinning sites to control the input and output position of the bits, while the purple squares (region III) highlight pinning sites that help pinning the first arriving domain wall. The input and output nanowires have a cross section $A$.

(b)–(e) Snapshots of the magnetization dynamics and functionality of the device depending on the first arriving domain wall. (f)–(i) Depinning dynamics explained by means of winding numbers, here applied to the OR-gate. Analog figures can be made for the AND-gate.
the core of an antivortex domain wall with negative [positive] core polarization moves downwards [upwards] while propagating, assuring that the output bit gets its predictable value.

An alternative way to understand the depinning dynamics is based on winding numbers. Conservation of total winding number [11, 21] ensures a stable and deterministic functionality of the AND- and OR-gates as outlined in figures 3(f)–(i) for OR-gate functionality. A transverse domain wall has winding number $-1/2$ at the vertex of its triangular shape and $+1/2$ at the other nanowire edge. In the AND-/OR-gates, the first arriving domain wall bit always pins with one winding center at the junction and the other at one of the outer notches. For identical input domain wall bits—panels (f) and (g)—the depinning results from the annihilation of winding numbers $+1/2$ and $-1/2$ near the junction. In panel (h), both domain walls have identical winding number $+1/2$ in the center near the junction, resulting in a repulsion of the winding centers. Here, depinning happens by splitting the $-1/2$ winding center of the last arrived domain wall bit into centers with winding number $-1$ and $+1/2$, i.e. by antivortex creation. The antivortex core (winding number $-1$) annihilates the two centers with winding number $+1/2$ near the junction. In panel (i) the depinning is caused by merging of the two centers with winding number $-1/2$ to an antivortex core (winding number $-1$) with polarization determined by the first arriving domain wall bit.

Since the functionality of the device depends on the domain wall bit arrival, it is important to control the initial bit location e.g. by introducing pinning sites (encircled in figure 3(a)) as well as controlling the propagation speed of the domain wall. When an identical current density, sufficiently large to depin the domain wall from the notch (see further), but smaller than $j_w$ is applied on both nanowires the domain wall bits propagate into the device. Slowing down the domain wall in one input arm enables one to control the arrival sequence. In figure 3(a), the domain wall in the bottom nanowire is slowed down by locally increasing the Gilbert damping to 0.03 in the green delineated area (figure 2(b)). As mentioned before, this can experimentally be accomplished by doping this area with rare-earth metals [16, 17].

At the junction region III, see figure 3(a), we used rectangular pinning notches and checked that their length and width can vary from 15.625 nm to 62.5 nm and 6.25 nm to 9.375 nm without changing the functionality of the logic gate. Moreover, electrical contacts are added to ensure that the current density in the output nanowire is the same compared to the input nanowires. The presented design operates for current densities $11 \text{ A} \mu\text{m}^{-2} < j < 14 \text{ A} \mu\text{m}^{-2}$. A notch is added in the output nanowire (region IV) to control the bit location at the output channel of the logic gate.

3.3. FAN-out

In a FAN-out element, an input bit is duplicated into two output bits. A possible design is similar to the AND/OR-gate presented above with the data now propagating from the right to left. The delay element in region I and the notches in region III become superfluous. Figure 4 shows snapshots of the magnetization dynamics at the (dis)junction. The opening angle at the junction is halved compared to the one in figure 3(a). In region III the transverse domain wall gets an increasing asymmetric shape with increasing nanowire width, see panel (a) and (b). At the (dis)junction, the domain wall splits introducing additional winding numbers $+1/2$ and $-1/2$. The part with vertex near the junction (winding number $-1/2$) moves on, while the other part initially pins, panels (c)–(f). Ultimately, magnetostatic interactions between the two domain walls depin the latter, panels (g)–(i). The presented design functions in the same current density range as the AND/OR gates.

4. Writing and reading devices

While the chirality based vortex domain wall logic [8] lacks an easily implementable mechanism to read and write the digital bit, reading and writing of the transverse domain wall bit is possible by measuring magnetization directions in the domain wall. To write a digital bit, one needs to define the output domain wall orientation (V or A) irrespective of its input value.
A possible design of a writing element is presented in figure 5. It has a symmetric pinning site—here triangular notches placed at both sides of the nanowire—which initially pins the domain wall, see top part of panels (a) and (b). Furthermore, the device contains electrodes with length \( L \) at the top and bottom edge which can locally apply a transverse current density \( j_y \) across the wire. When applying a current \( j_x \) larger than the depinning current, the domain wall bit propagates through the wire passing the region between the electrodes while also tilting the magnetic moments within the domain wall out-of-plane [18]. Here, the additional current density \( j_y \) stabilizes domain walls bits with magnetization orientation in the same direction of the current \( j_x \), see figure 5(a), and destabilizes domain wall bits with opposite magnetization orientation, see figure 5(b). This corresponds to delivering a torque pushing the tilted moments back in-plane (shifting the Walker breakdown \( j_w \) to higher current densities \( j_x \)) and pushing them further out-of-plane (shifting \( j_w \) to lower \( j_x \)) respectively: in the case depicted in panel (b), the magnetization inside the domain wall reverses, changing also the V-shape of the domain wall (digital 1) into the A-shape (digital 0). The reversal happens by means of intermediate antivortex creation, similar to what happens above the Walker breakdown. Hence, a transverse current density \( j_x \) can set the domain wall orientation (the bit) independent of its initial state.

The magnetization orientation in a domain wall bit not only depends on the domain wall shape (V or A), but also on the head-to-head or tail-to-tail nature of the wall. This is to be taken into account when applying \( j_x \). Figure 5(c) shows the direction of \( j_x \) to get the desired output. In the writing device, a Magnetic Tunnel Junction (MTJ) determines the magnetization orientation in the domain left of the pinned domain wall bit to distinguish between a head-to-head or tail-to-tail domain wall. Furthermore, since the bit reverses while propagating, the length \( L \) of the electrodes has to be tailored to sustain the complete reversal process. The minimum length depends on the current density \( j_x \) driving the domain wall along the nanowire and on the amplitude of the current density \( j_y \) destabilizing the domain wall. Figure 5(c), shows the minimum \([j_x - L]\) values that guarantee a correct functionality for the writing device for various transverse current densities \( j_y \). When applying larger transverse currents \( j_y \), the minimum values for \( L \) and \( j_x \) shift to lower values as can be expected. In practice, it is challenging to apply currents \( j_x \) and \( j_y \) independent from each other. As an alternative, pulsed currents \( j_x \) and \( j_y \) succeeding each other can be applied, thereby exploiting the inertia of the moving domain wall. This was confirmed with simulations: for example, when applying a pulse of \( j_x = 12 \, \text{A} \, \text{µm}^{-2} \) for 5 ns, thereby transporting the domain wall between electrodes with length \( L = 1500 \, \text{nm} \), succeeded by a pulse of \( j_y = 2.5 \, \text{A} \, \text{µm}^{-2} \) for 5 ns, a correct functionality of the alternative writing element was observed. The design robustness is assured when the electrodes are oversized given a working current density \( j_x \).
To read a digital bit, one needs to determine its shape (V or Λ). Figures 6(a) and (b) present a possible design for a reading element. Similar to the writing element, this design has a symmetric pinning site to initially pin the domain wall, see top part of panels (a) and (b). Next to a MTJ to determine the magnetization orientation in the domain left of the pinned domain wall (MTJ$_1$), there is a MTJ centered on the pinning site to distinguish between the magnetization orientation of a positively and negatively polarized domain wall (MTJ$_2$). Combining the information extracted from these two MTJs unambiguously renders the bit value of the pinned domain wall as illustrated in panel (c). Instead of using two MTJs, one can also distinguish between a V and Λ transverse domain wall shape by measuring the resistivity when the domain wall is pinned at a triangular notch placed at one side of the nanowire. This has been demonstrated experimentally [22]. However, since such a readout scheme relies on detecting extremely small signals, the signal-to-noise ratio is much worse than in the case of using MTJs. Anyway, this readout only needs to be realized when interfacing with other logic and will be reduced when more magnetic logic is integrated.

5. Discussion

The numerical proofs-of-principle presented here demonstrate that it is theoretically feasible to make an all-magnetic ICT platform in which the digital data is stored and processed under the same magnetic representation. As all devices have identical input and output cross sectional dimensions, digital networks can be designed in which multiple digital elements are combined. This way, a FAN-out element can duplicate the digital bits stored in a wire of an in-plane racetrack memory in order to perform digital operations on it. Contrary to magnetic field driven elements, our current driven concepts enable the data to easily propagate through bended nanowires [23], resulting in little geometrical restrictions when connecting the elements. Moreover, the use of electrical currents makes it possible to process multiple successive data bits in one and the same nanowire network.

Similar to the racetrack memory, the bit location within nanowire networks can be controlled by introducing pinning sites combined with the use of current pulses. Figure 7 presents the maximum current for which symmetrically placed triangular notches with depth $d$ pin the transverse domain wall. Domain wall velocity versus applied current density for a nanowire with width 100 nm and width 50 nm. Both wires are 10 nm thick.

![Figure 6](image1.png)

(a) and (b) Snapshots illustrating the functionality of a possible reading element able to discriminate between V- and Λ-shaped domain walls. It contains a symmetrical pinning site (highlighted with black circles) and two MTJs. MTJ$_1$ measures the magnetization direction in the domain left from the domain wall, while MTJ$_2$ measures the polarization of the domain wall. (c) Table summarizing the value of the bit depending on the magnetization measured by MTJ$_1$ and MTJ$_2$.

![Figure 7](image2.png)

(a) Maximum current density for which symmetrically placed triangular notches with depth $d$ pin the transverse domain wall. (b) Domain wall velocity versus applied current density for a nanowire with width 100 nm and width 50 nm. Both wires are 10 nm thick.
Numerical designs are relatively robust with respect to changes to the specific shape and the depth of the pinning sites, pinning is known to have a stochastic character [25, 26]. This can impede the implementation of the presented technology, equally as all other magnetic nanowire based digital technologies, and is subject to various specific studies [22, 23, 27–29].

An alternative pinning approach could be a local increase of material disorder. This gives rise to a collective pinning mechanism and is less constrained by the lithography limitations, making the proposed logic schemes cheaper to implement, while also offering better miniaturization possibilities [15, 30]. One way to create such pinning sites is by local implantation of chromium ions [31, 32]. The strength of the pinning potential is then determined by the chromium ion fluence.

For the presented proofs-of-concept, the AND-/OR-gates have the longest bit run-through time of about 100 ns at high current density $j_m \sim 1.7$. Combined with a 50 ns low current density ($j_m$) time window to pin the domain walls at predefined locations, this leads to an estimated pulse length of about 150 ns, and thus an envisaged clock speed of 66 MHz. Contrary to the chirality based domain wall concept [8], the presented technology can be miniaturized since also in smaller nanowires the transverse domain wall remains stable. Figure 7(b) shows how halving the nanowire width from 100 nm to 50 nm (and thus also halving the lateral dimensions) has only an impact on the Walker breakdown current $j_m$, but not on the domain wall velocity below it. Hence when downsizing in-plane dimensions of the presented concepts (tailoring again notch depths, electrode lengths, etc.), run-through times are downscaled proportionally. Consequently, envisaged clock speeds scale linearly with miniaturization.

Similar to other electric current based magnetic domain (wall) technologies, the proposed concepts suffer also from serious Joule heating, making the experimental implementation of current driven domain (wall) technologies in general challenging. However, controlled current induced domain wall motion has been demonstrated experimentally by several groups, see [33] and references therein. Moreover, switching of the transverse domain wall orientation above the Walker breakdown is experimentally observed at relatively low current densities compared to ideal nanowires [34, 35]. Vanhaverbeke et al [34] and Heyne et al [35] observe the transformations above the Walker breakdown respectively at about 1.7 A $\mu$m$^{-2}$ and at an even lower current density of about 1 A $\mu$m$^{-2}$. Current studies to minimize Joule heating comprise optimization of current pulse profiles [36]. Alternatively, concepts based on high PMA materials could be developed since current induced domain wall motion in such systems is observed at significantly lower current densities [37–39]. However, the domain wall chirality should not be fixed like in some concepts of PMA racetrack memory discussed in [40]. Another aspect characteristic to nanowires with transverse domain walls is the mutual interaction between domain walls in nanowires due to their stray fields [41, 42]. In the design of the AND/OR-gates and the FAN-out, these are taken into account. Also in the design of complete (parallel) logic networks these mutual interactions need to be properly addressed.

6. Conclusions

We have introduced a digital logic and memory concept in which the binary data is stored in the magnetic transverse domain walls rather than the magnetic domains existing in in-plane magnetized nanowires with reduced cross-sectional dimensions. Numerical proofs-of-concept are presented for a NOT-, OR- and AND-gate, a FAN-out as well as a reading and writing device. Since all designs are current driven and have identical cross-sectional dimensions at the input and output nanowires, the devices can be easily combined to logic networks that are compatible with the in-plane racetrack memory concept. Contrary to field driven vortex domain wall based technologies, the transverse domain wall bit remains stable when downsizing the technology. While the sub-optimal designs presented here have an envisaged clock speed of about 66 MHz, clock speeds are expected to scale linearly with miniaturization. This opens opportunities towards a future all-magnetic high-density computing technology in which the data is stored and processed under the same magnetic representation.

Acknowledgments

Research funded by a PhD grant of the Agency for Innovation by Science and Technology (IWT). B Van de Wiele is financially supported by the Flanders Research Foundation (FWO). Financial support was also provided by Ghent University (BOF-project 01J16113).

References


[37] Koyama T et al 2011 Observation of the intrinsic pinning of a magnetic domain wall in a ferromagnetic nanowire Nat. Mater. 10 194–7

[38] Koyama T et al 2012 Current-induced magnetic domain wall motion below intrinsic threshold triggered by walker breakdown Nat. Nanotechnol. 7 635–9


